

Description:

This document demonstrates how to use Intersil's ISL5416 3G Quad Programmable Down Converter for CDMA2000 and W-CDMA (UMTS) cellular applications.

The block diagrams in this application note show the data path through a single channel's filter blocks: the CIC, FIR1, FIR2 and resampler (if enabled). Not shown are the NCO and mixer blocks which precede the CIC filter. The configurations referenced in this application note make use of only channel 2 — channels 0, 1 and 3 may be copied from channel 2 to provide up to 4 receivers if desired. The inputs are set to bus C (eval board connector J3) and expect 2's complement format.

For standalone demonstration on the evaluation board (no external inputs or clocks), set the channel 2 input to the microprocessor test input register with the ENI bit enabled. This input appears to the mixer as a DC source, providing the NCO output as a sinusoidal source to the filter chain and allowing the filter chain to be swept (see tracing out a filter response below).

General procedure for loading and running a configuration:

1. Load the configuration files (main menu item 18). The configuration files for the examples in this application note are included with the ISL5416 Evaluation Board software in the configs directory.
2. Change the evaluation board port if needed (main menu item 1). These configurations assume the evaluation board is addressed as board # 0.
3. Initialize the board (main menu item 17).
4. Compute the register files (main menu item 10).
5. Download register files to ISL5416 (main menu item 12).
6. To display output data, select Run and Display mode (main menu item 13). Exit this mode by pressing "9".

Tracing out a filter response:

When a channel's input is set to the microprocessor test input register with ENI enabled, the channels sees a DC input and the mixer output is simply the NCO's sinusoidal outputs scaled by the DC value. A filter frequency response can be found by stepping the NCO frequency and measuring the output magnitude at each step. This is exactly what is done in the "Filter Sweep" option of the Data Collection and

Display Menu (main menu item 11, then item 3). Details on doing this frequency sweep are provided in the evaluation board user's manual in the "Data Collection and Display Menu" section. The end result is a file called "sweep.imp" containing frequency vs. output magnitude. A plot can be made in MATLAB using the following code:

```
a=fgetimp('sweep.imp');
plot(a(:,1), a(:,2)-max(a(:,2))); grid
```

The plots provided in the following pages were obtained in this manner. Function fgetimp is provided in the included MATLAB tools for modeling the ISL5416 CIC and FIR filter responses.

A more interactive tracing of the filters can be done in the Run and Display mode. In this mode, pressing the right and left arrow keys steps the carrier NCO frequency up and down. The real-time FFT displays the output spectrum, showing not only the magnitude of the frequency response at the input frequency but also the presence of noise and images. A procedure for obtaining a trace of the filter in Run and Display mode is as follows:

1. Load a configuration and enter Run and Display mode using the procedure provided on the left.
2. Step the NCO center frequency to 0 (DC) using the left and right arrow keys. When the frequency is close to DC, press the down arrow at least 8 times. This sets the NCO step size to the smallest step. Continue stepping the NCO frequency until it is approximately 0 (don't worry that the step size may not permit a frequency of exactly 0).
3. Press "1" to toggle the blue peak trace on (if not already enabled).
4. Press "4" to reset (zero) the peak trace.
5. Press "6" to toggle to AGC loop 2 ("AGC 2"). In all the examples included (and in all default configurations), the AGC loop gain 2 slew rates are set to 0 dB/output (AGC is disabled). This prevents the AGC from counteracting the effects of the filter.
6. Press and hold the right (or left) arrow key to decrease (increase) the frequency applied to the CIC's input. The peak trace will hold the filter's response. The span of the FFT display is $-(\text{output rate} / 2)$ to $(\text{output rate} / 2)$. The NCO frequency should be increased (or decreased) past the edge of the FFT display to see the effects of signals well into the stop band. While stepping the NCO frequency, look for noise or images which would indicate a problem in the configuration.

The figure below is a screen shot of Run and Display mode being used to trace out the filter response of the included cdma2k61.416 configuration (Configuration 1 below). The NCO frequency was stepped up from DC to about 5 MHz, showing the filter response to pass band and stop band signals. The span of the FFT below is -2.4576 MHz to

2.4576 MHz with DC in the center. The largest out-of-band image is about 58 dB below the pass band and occurred at around 595 kHz (the edge of the pass band). The input frequency may be stepped all the way up to $F_s/2$, where F_s is the A/D sample rate. Note that "Center Freq" below is the negative of the carrier NCO frequency.

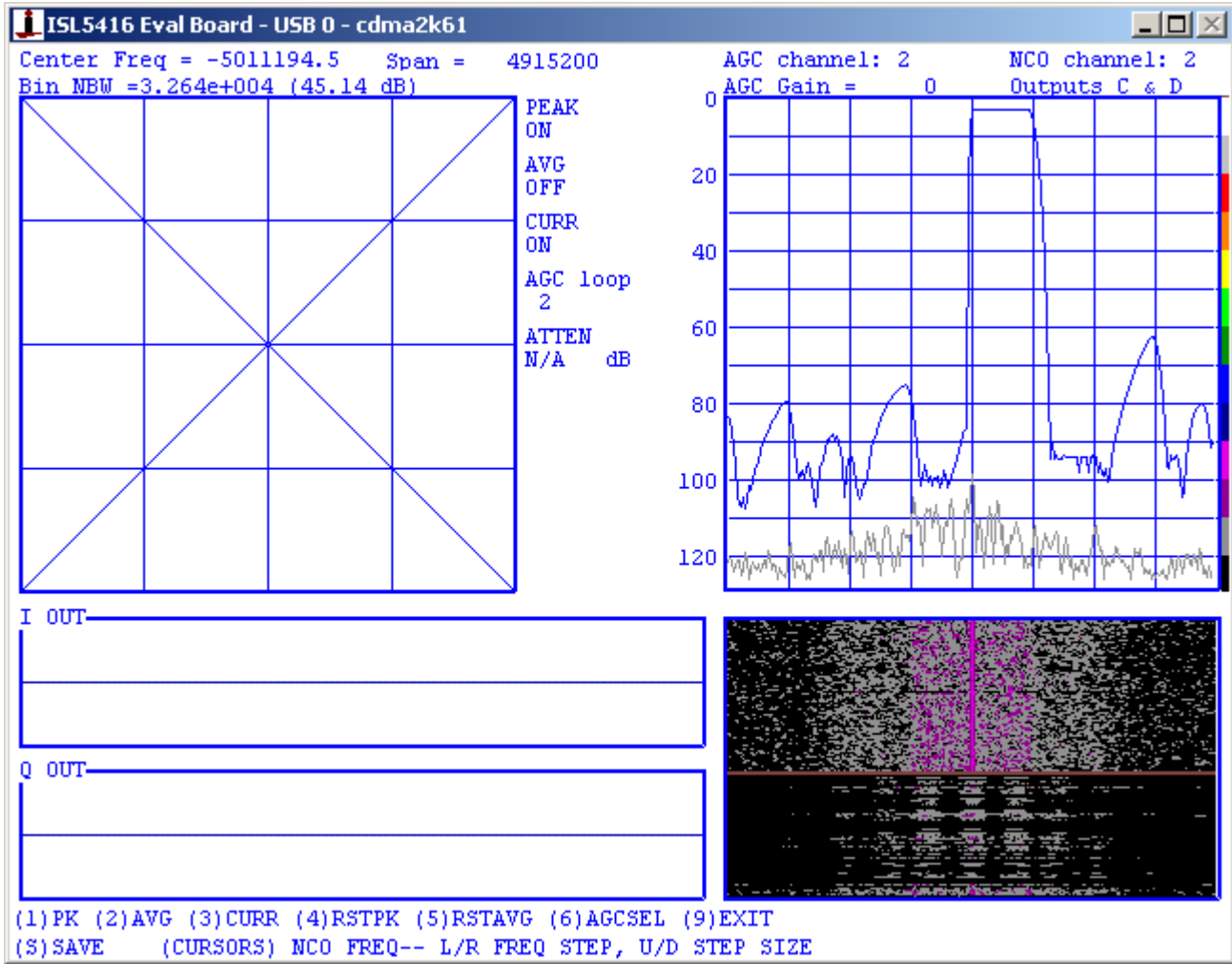


FIGURE 1. TRACING THE CDMA2K61 CONFIGURATION'S FILTER RESPONSE IN RUN AND DISPLAY MODE. THE NCO FREQUENCY WAS STEPPED FROM DC TO JUST OVER 5 MHz WITH THE PEAK TRACE ON.

Configuration 1 – CDMA2000-1xRTT

Configuration Filename: CDMA2K61.416

Input Rate: 61.44 (50x)

Output Rate: 4.9152 MSPS (4x)

Output Format: 24 bit I on time slot 0 with I(23:8) on COUT and I(7:0) on DOUT(15:8), likewise for Q on time slot 1.

The block diagram of the implementation is shown in Figure 2 below.

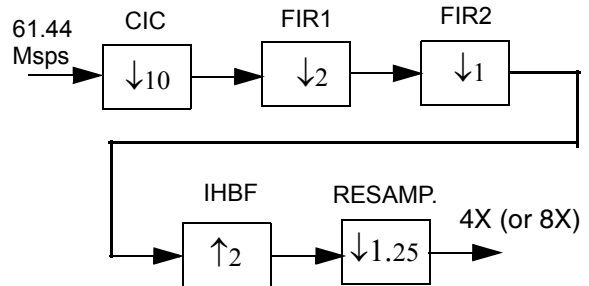


FIGURE 2. CONFIGURATION 1 FILTER BLOCK DIAGRAM

The chosen CIC decimation of 10 in this configuration yields a first alias level of about -94.8 dB with the 2-sided signal bandwidth taken as 1.25 MHz.

FIR1 is a 32-tap FIR filter, decimating by 2. Its role is to compensate for the CIC droop and do the “rough” filtering. Its frequency response is provided in Figure 3. FIR 2 is a 64-tap filter, decimating by 1. The output rate of the FIR2 is 3.072 Msps, or 2.5x. Therefore, the IHBF is enabled to increase the rate to 5x. The resampler is also enabled to achieve the final desired rate of 4.9152 Msps (4x). If required, the resampler can increase the final output rate to 8x or more.

PARALLEL OUTPUTS:

This configuration’s output is 24 bits of I data on time slot 0 with I(23:8) on COUT and I(7:0) on DOUT(15:8), and similarly for Q on time slot 1. Other parallel output options include:

- 16 bit I data on COUT and 16 bit Q data on DOUT during a single time slot
- 16-bit I data to the COUT bus on slot 0 and 16-bit Q data to COUT during slot 1 (multiplexing I and Q data onto a single 16 bit bus)
- 8 bit I on COUT(15:8) and 8 bit Q on COUT(7:0) (I and Q together on the same 16 bit bus and on the same time slot)

See the Output Routing Menu in the evaluation board software for details in configuring the parallel outputs.

SERIAL OUTPUTS:

The DOUT bus can be programmed to work as a serial output, providing 2 serial data outputs per channel.

The overall decimation of $50X / 4X = 12.5$ allows for a maximum of 12 bits per sample per serial output. This allows, for example, 12 bit I on SD1C and 12 bit Q on SD2C or 6 bit I followed by 6 bit Q on SD1C.

Note that the ISL5416 eval board software does not determine symbol or chip timing - it only plots the I and Q outputs, I vs. Q, and FFTs of 256 point captures. To obtain a constellation plot, the symbol timing on the ISL5217 upconverter can intentionally be offset by about 1 Hz so that the ISL5416 eval board slices at exactly the middle of the symbol once a second. The tightness of the constellation points can be used to judge the match between the transmit and receive filters. Further analysis may be done by capturing the output data to a file and importing it into an application such as Matlab. See the “Data Collection and Display Menu” section of the evaluation board user’s manual for more information on this.

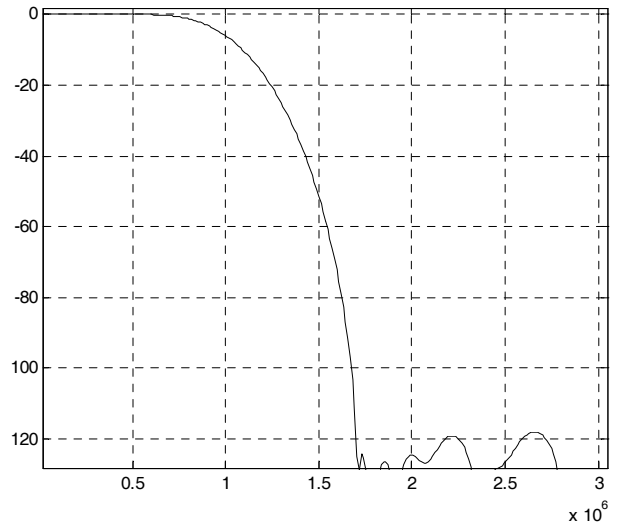


FIGURE 3. CONFIGURATION 1: FIR1 (32 TAPS)
FREQUENCY RESPONSE (dB VS. FREQUENCY)

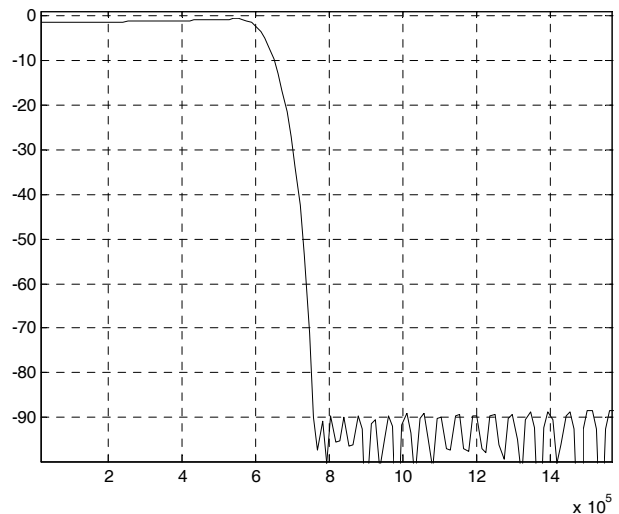


FIGURE 4. CONFIGURATION 1: FIR2 (64 TAPS)
FREQUENCY RESPONSE (dB VS. FREQUENCY)

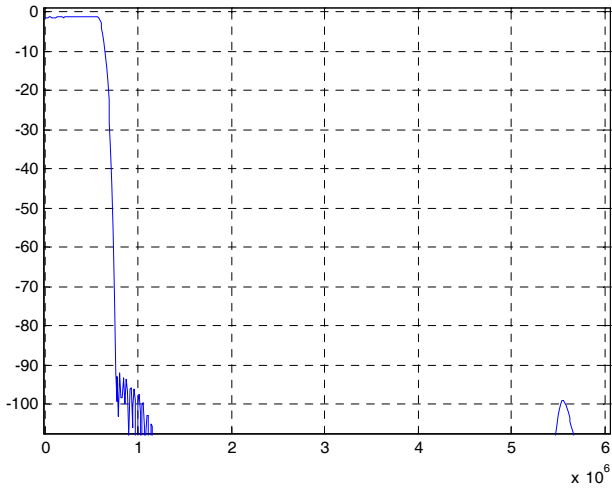


FIGURE 5. CONFIGURATION 1: COMBINED RESPONSE OF CIC, FIR1 AND FIR2 (dB VS. FREQUENCY).

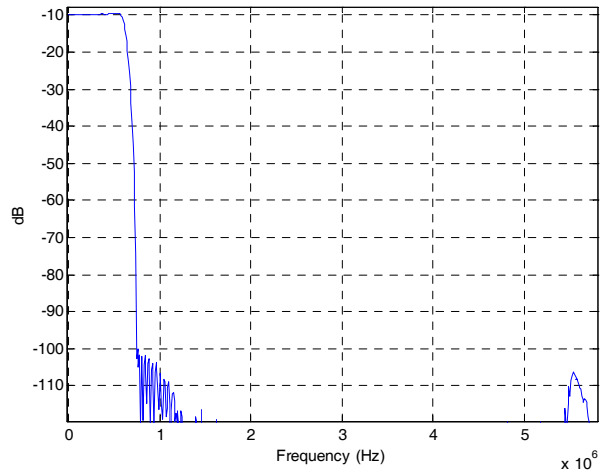


FIGURE 6. CONFIGURATION 1: SWEEP OF THE FILTER AS IMPLEMENTED ON THE ISL5416 EVAL BOARD (dB VS. FREQUENCY), DC TO 6 MHz.

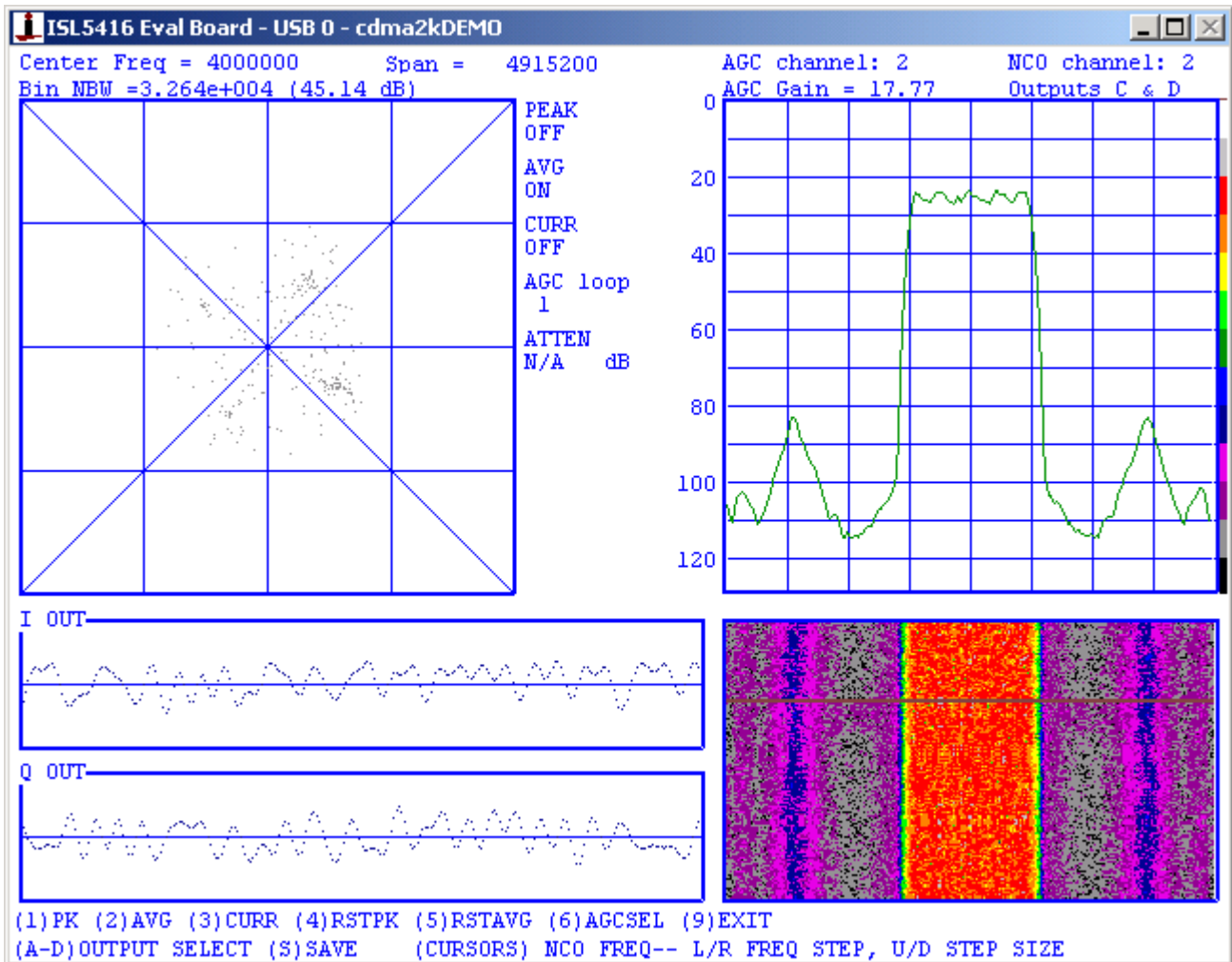


FIGURE 7. CONFIGURATION 1: ISL5416 EVAL BOARD SOFTWARE IN RUN AND DISPLAY MODE

Configuration 2 – CDMA2000-1xRTT

Configuration Filename: CDMA2K80.416

Input Rate: 80 Msps

Output Rate: 4.9152 MSPS (4x)

Output Format: 24 bit I on time slot 0 with I(23:8) on COUT and I(7:0) on DOUT(15:8), likewise for Q on time slot 1.

The block diagram of the implementation is shown in Figure 8 below.

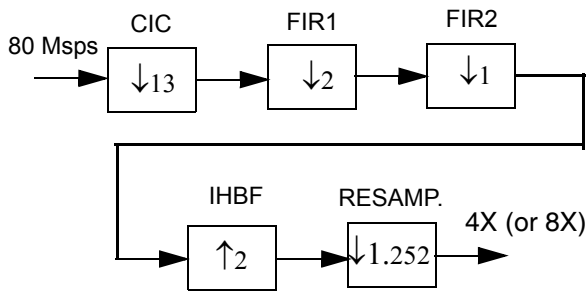


FIGURE 8. CONFIGURATION 2: FILTER BLOCK DIAGRAM

The chosen CIC decimation of 10 in this configuration yields a first alias level of about -95 dB with the 2-sided signal bandwidth taken as 1.25 MHz.

FIR1 and FIR2 use the same filter coefficients as Configuration 3. The only differences are the CIC decimation (10 for 61.44 MSPS and 13 for 80 MSPS to present FIR1 with a rate of about 6.144 MSPS) and the presence of the IHBF and resampler here to give an output rate of exactly 4.9152 MSPS (4X). If desired, the resampler can increase the final output rate to 8x or more.

The output format is the same as that of Configuration 1. Refer to Configuration 1 for examples of available parallel and serial output formats.

A filter sweep plot is shown in Figure 9. This is an actual plot of the ISL5416's output magnitude as the input frequency is swept from DC to 6MHz.

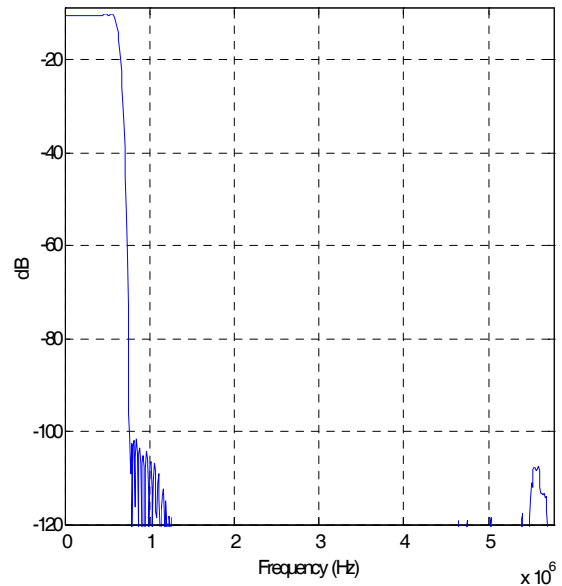


FIGURE 9. CONFIGURATION 2: SWEEP OF THE FILTER AS IMPLEMENTED ON THE ISL5416 EVAL BOARD (dB VS. FREQUENCY), DC TO 6 MHz.

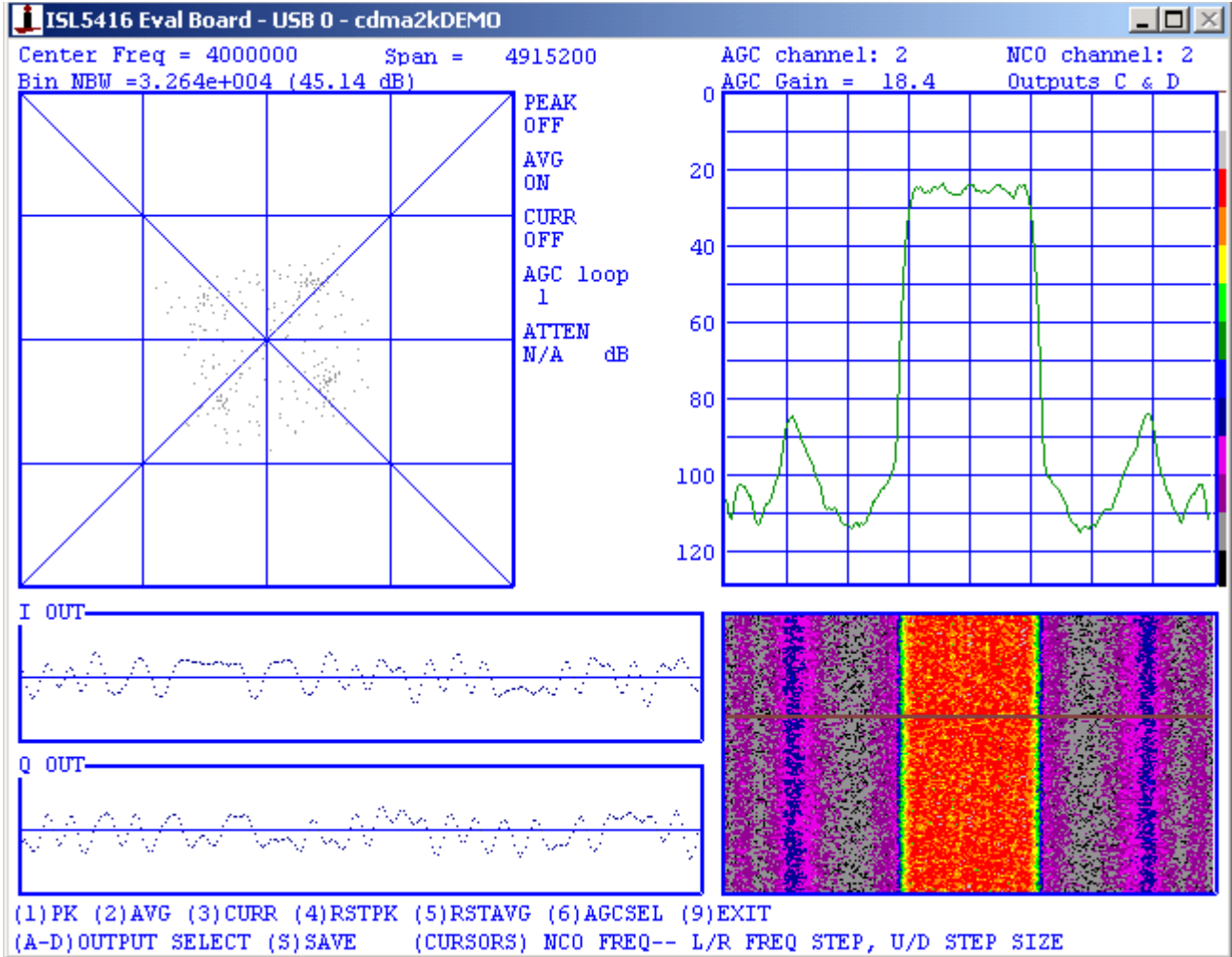


FIGURE 10. CONFIGURATION 2: ISL5416 EVAL BOARD SOFTWARE IN RUN AND DISPLAY MODE

Configuration 3 – W-CDMA (UMTS)

Configuration Filename: 3G6144.416

Input Rate: 61.44 Msps (16x)

Output Rate: 15.36 MSPS (4x)

Output Format: 24 bit I on time slot 0 with I(23:8) on COUT and I(7:0) on DOUT(15:8), likewise for Q on time slot 1.

The block diagram of the implementation is shown in Figure 11 below.

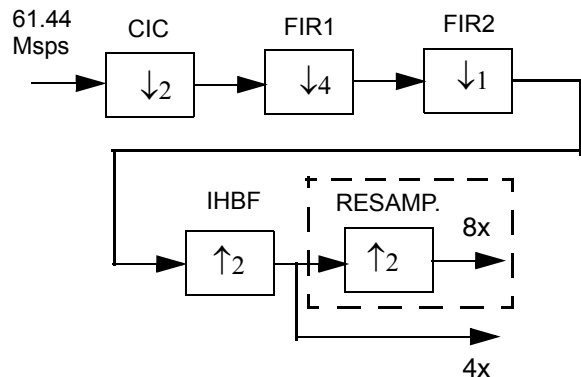


FIGURE 11. CONFIGURATION 3: FILTER BLOCK DIAGRAM

The chosen CIC decimation of 2 in this configuration yields a first alias level of -100 dB for a two-sided bandwidth of 3.84 MHz.

FIR1 is a 31-tap half band filter decimating by 4. It compensates for the CIC droop and provides filtering for the decimation by 4. Its frequency response is provided in Figure 12. FIR2 is a 64-tap RRC filter ($\alpha = 0.22$) decimating by 1. The output rate of FIR2 is 7.68 Msps. Therefore, the IHBf is enabled to increase the rate to 15.36 Msps (4x). The resampler could be enabled to achieve the rate of 30.72 Msps (8x) if desired.

The output format is the same as that of Configurations 1. Refer to Configuration 1 for examples of available parallel and serial output formats.

Figure 14 shows the composite response of the CIC, FIR1 and FIR2 filters as simulated in Matlab. A filter sweep is provided in Figure 15. This is an actual plot of the ISL5416's output magnitude as the input frequency is swept from DC to 15.36 MHz.

Figure 16 is a screen shot from the ISL5416 eval board software while receiving a W-CDMA (UMTS) signal from an ISL5217 quad programmable upconverter eval board. The four-point constellation is clearly visible in the I vs Q box, along with randomly scattered points from the mid-symbol samples. This plot was achieved by offsetting the ISL5217's symbol timing by about 0.1 Hz and capturing the screen when the symbol slicing was at the best position.

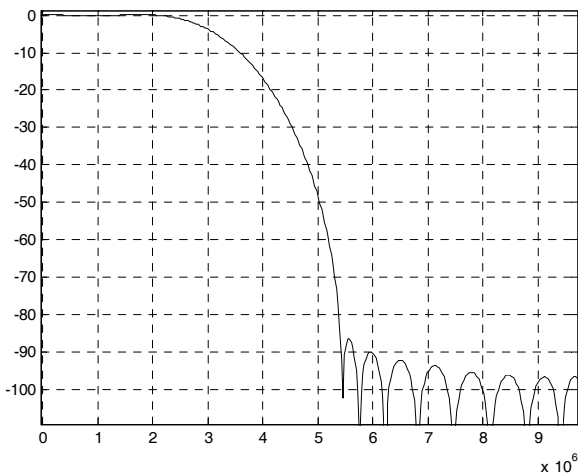


FIGURE 12. CONFIGURATION 3: FIR1 (31-TAP-HBF) FREQUENCY RESPONSE (dB VS. FREQUENCY)

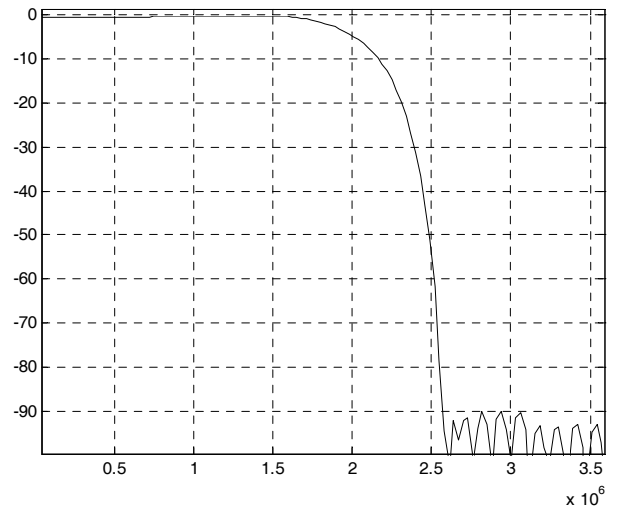


FIGURE 13. CONFIGURATION 3: FIR2 (64-TAP RRC) FREQUENCY RESPONSE (dB VS. FREQUENCY).

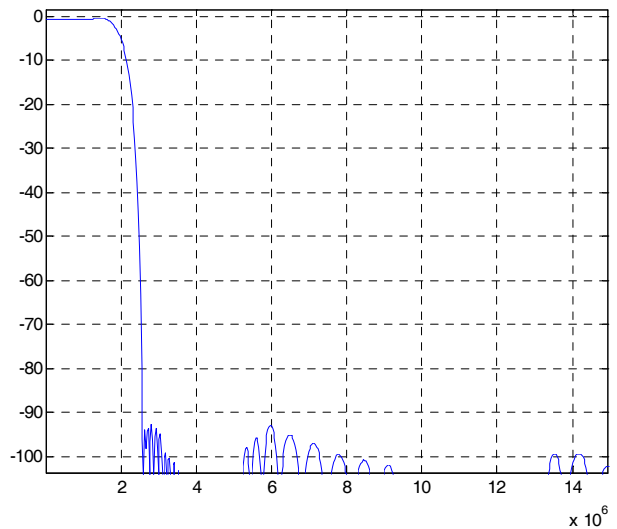


FIGURE 14. CONFIGURATION 3: COMBINED FREQUENCY RESPONSE OF CIC, FIR1 AND FIR2 (dB VS. FREQUENCY)

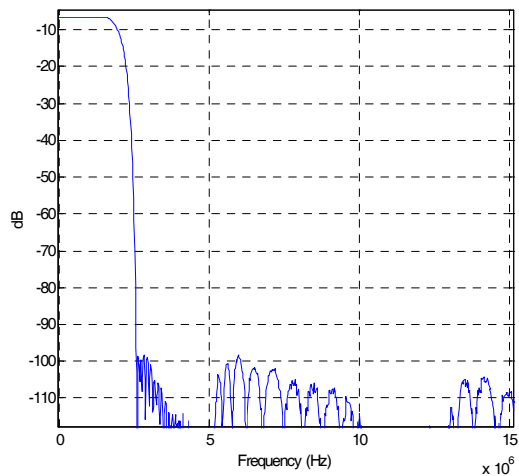


FIGURE 15. CONFIGURATION 3: FREQUENCY SWEEP OF THE FILTERS AS IMPLEMENTED ON THE ISL5416

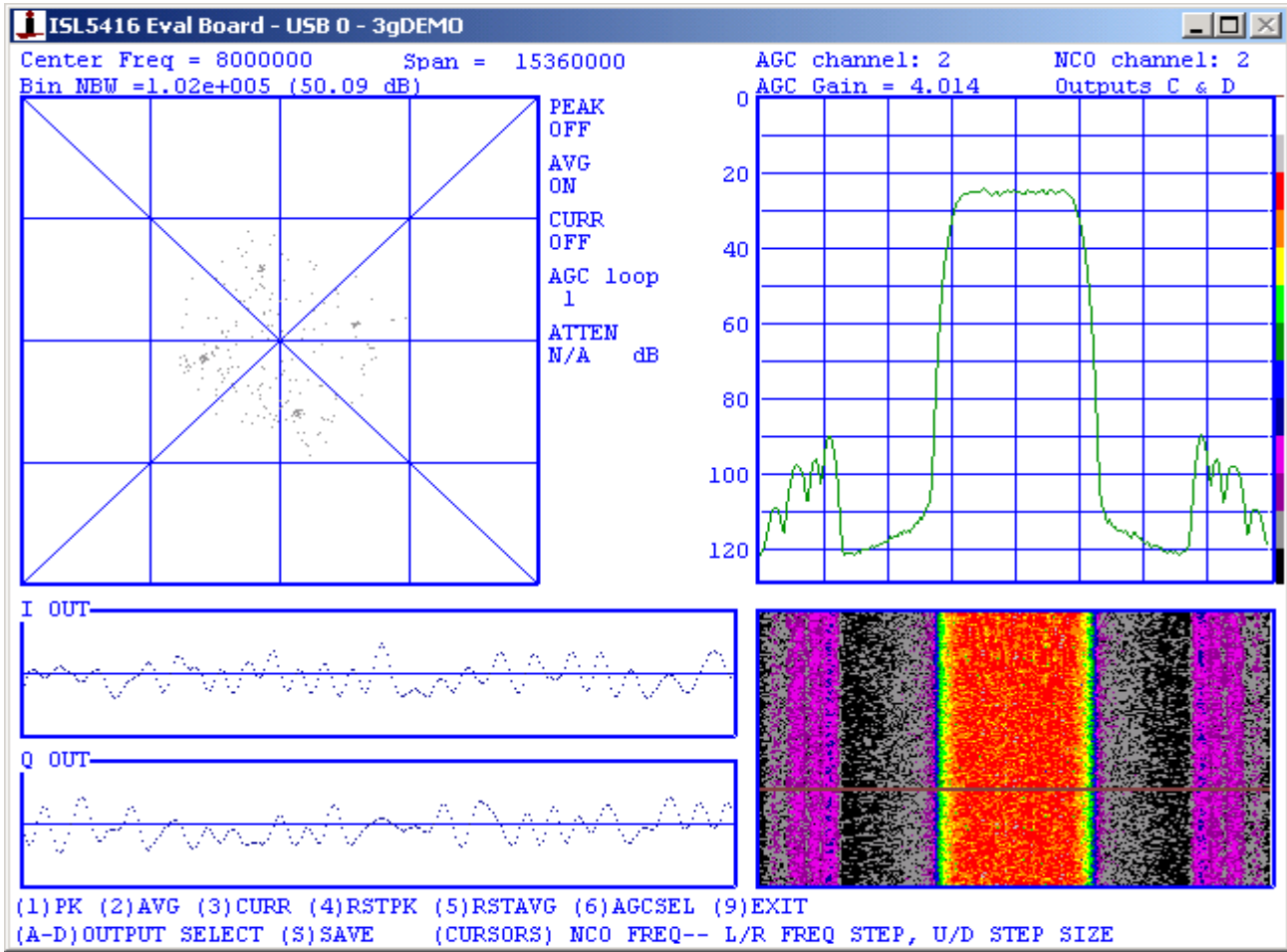


FIGURE 16. CONFIGURATION 3: EVAL BOARD SOFTWARE SCREEN SHOT

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